TEXAS INSTRUMENTS

TLV2553EVM and TLV2556EVM

User's Guide

March 2003

Data Acquisition Products

SLAU102

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 5 V and the output voltage range of 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TLV2553/6EVM 12−bit serial analog to digital evaluation board. A complete circuit description as well as schematic diagram and bill of materials is included. Please contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—EVM Overview
- ❏ Chapter 2—Digital Interface
- ❏ Chapter 3—Power Supply
- ❏ Chapter 4—Getting the Most From Your EVM
- ❏ Chapter 5—TLV2553/6EVM Bill of Materials
- ❏ Chapter 6—TLV2553/6EVM Board Layout and Schematic

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

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Data Sheets:	**Literature Number:**
TLV2553	SLAS354B
TLV2556	SLAS355A
OPA132	SBOS054
REF02	SBVS003A

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademarks

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Chapter 1

EVM Overview

The TLV2553EVM and the TLV2556EVM are 11-channel, 12-bit analog-to-digital converter boards based on the TLV2553 ADC or TLV2556 ADC. The ADC uses a synchronous serial interface which can be simply interfaced to many microcontrollers using the SPI protocol.

The EVM also incorporates a stable voltage reference and operational amplifier, to ensure a low-noise voltage reference for the ADC.

Topic **Page**

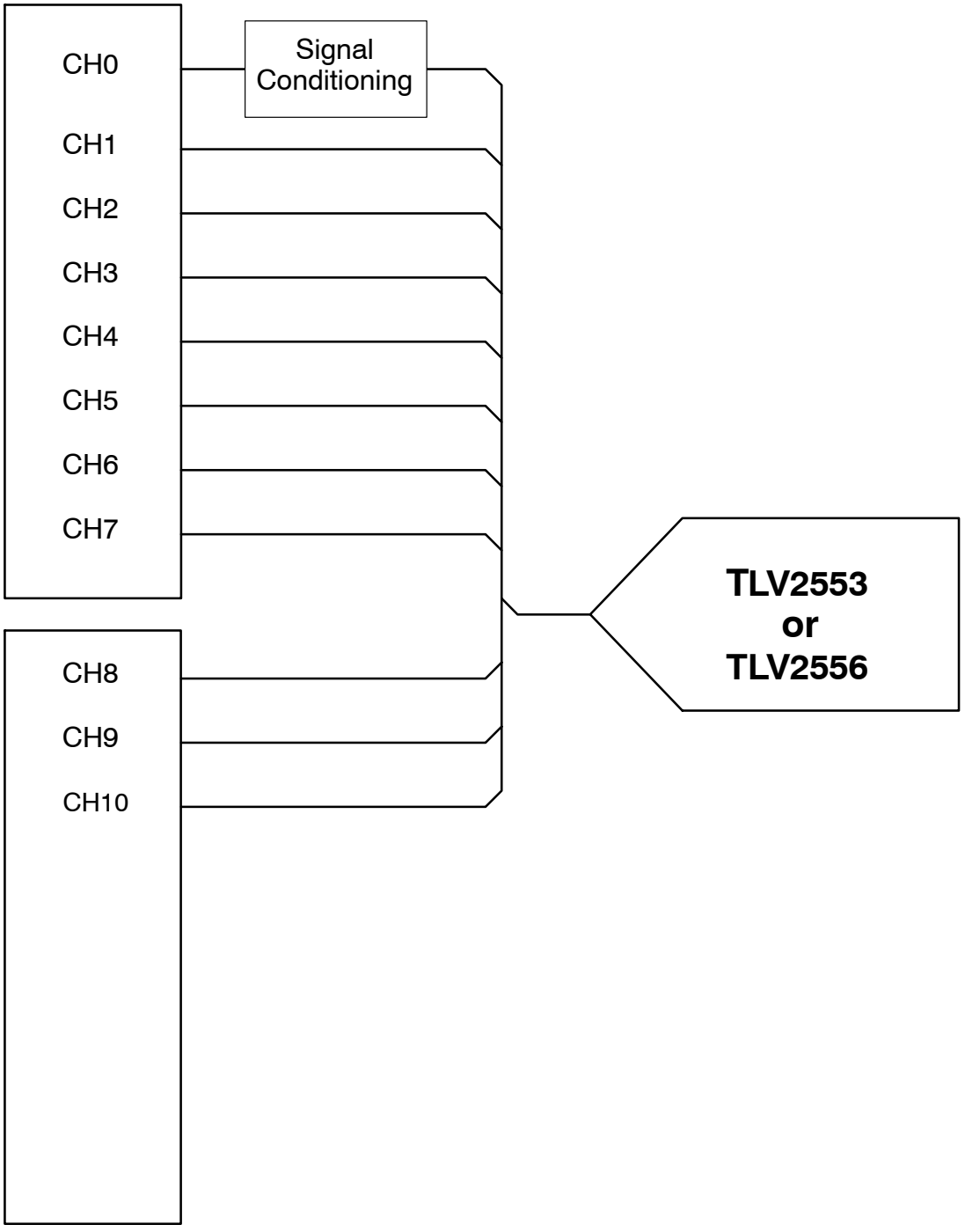
1.1 Features

- Evaluation board featuring either the TLV2553 ADC (order TLV2553EVM) or the TLV2556 ADC (order TLV2556EVM)
- Onboard reference, with recommended buffer circuitry
- Suggested signal conditioning circuitry for one channel only

1.2 Analog Interface

A block diagram for the analog interface of the EVM is shown in Figure 1−1.

Figure 1−1. Analog Interface Block Diagram



The channels are arranged to comply with the EVM standard developed for data converters. This standard defines eight channels of analog I/O on each EVM module.

Since these ADCs possess 11 channels, the standard module width is doubled to incorporate all 11 channels in a convenient form.

1.3 Signal Conditioning

The facility exists for the signal connected to channel 0 to be conditioned by an operational amplifier. The amplifier present on the EVM operates from a dual power supply and is configured with a gain of 1.

If signal conditioning is not required, it can easily be bypassed by a shorting bar at W6.

1.4 Single Supply Operation

Should the user wish to operate the amplifier from a supply single rail, this is also possible by simply removing the dual supply amplifier and replacing it with a suitable single supply alternative, for example the OPA353.

The suggested procedure is detailed below:

- ❑ Carefully desolder amplifier, U1
- ❑ Replace with a suitable single-supply alternative, for example TI part number OPA353UA
- ❑ Install appropriate resistor at R11
- ❑ Install appropriate capacitor at C15
- ❑ Install shorting bar at W1

1.5 Physical Pinout Description

Samtec part numbers SSW−110−22−F−D−VS−K and TSM−110−01−T−DV−P provide a convenient 10-pin dual row header/socket combination at P1. This header/socket provides access to the analog input pins of the TLV2553/6.

Consult Samtec at www.samtec.com or 1−800−SAMTEC−9 for a variety of mating connector options.

Table 1−1. Analog Input Connector

Pin Number		Signal	Description
Header	**Socket**		
P1.2	J1.2	CH0	Channel 0 input, can be direct from P1/J1 connector or through op-amp
P1.4	J1.4	CH1	Channel 1 input, direct from P1/J1 connector
P1.6	J1.6	CH2	Channel 2 input, direct from P1/J1 connector
P1.8	J1.8	CH3	Channel 3 input, direct from P1/J1 connector
P1.10	J1.10	CH4	Channel 4 input, direct from P1/J1 connector
P1.12	J1.12	CH5	Channel 5 input, direct from P1/J1 connector
P1.14	J1.14	CH6	Channel 6 input, direct from P1/J1 connector
P1.16	J1.16	CH7	Channel 7 input, direct from P1/J1 connector
P1.18	J1.18	REF−	External reference negative input
P1.20	J1.20	REF+	External reference positive input

Table 1−2. Analog Input Connector

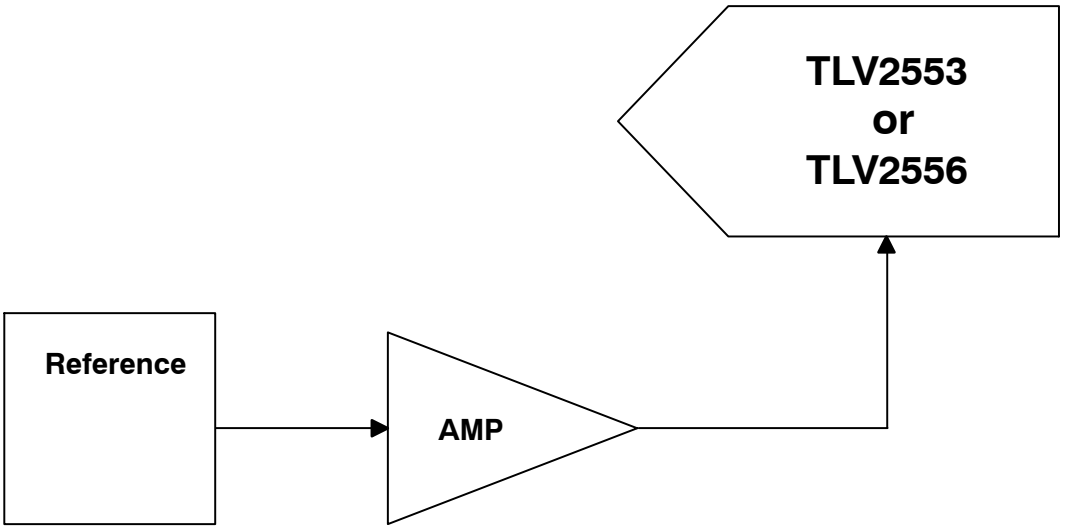
Pin Number		Signal	Description
Header	**Socket**		
P2.2	J2.2	CH8	Channel 8 input, direct from P2/J2 connector
P2.4	J2.4	CH9	Channel 9 input, direct from P2/J2 connector
P2.6	J2.6	CH10	Channel 10 input, direct from P2/J2 connector
P2.8	J2.8	Reserved	
P2.10	J2.10	Reserved	
P2.12	J2.12	Reserved	
P2.14	J2.14	Reserved	
P2.16	J2.16	Reserved	
P2.18	J2.18	Reserved	
P2.20	J2.20	Reserved	

1.6 Reference Voltage

The accuracy of conversion from a SAR ADC depends directly upon the accuracy of the reference voltage. It is very important, therefore, that the reference be stable, accurate, and low drift.

A block diagram of the suggested circuit is shown in Figure 1–2.

Figure 1–2. Circuit Diagram



The ADC reference pin presents a dynamic capacitive load to the amplifier. The voltage supplied to the ADC must be capable of driving this dynamic load properly, ensuring that the reference remain stable regardless of load.

1.7 Configuration Options

There are a number of options available by shorting jumpers. These are detailed in Table 1–3.

Table 1–3. Configuration Options

Reference Designator	Description	Factory Set Condition	
		1–2	2–3
W1	Single supply operation	Installed (see Note)	
W2	Select positive voltage reference	Onboard reference, +4 V	Reference via P1.20
W3	Select negative voltage reference	Onboard reference, 0 V	Reference via P1.18
W4	Select negative supply for op amp	–Vs	AGND (0 V)
W5	Select positive supply for op amp	+Vs	+Vcc (+5 V)
W6	Select signal source for channel 0	Signal is via op amp	Signal is directly from P1.2

Note: Dual supply op amp is installed. W1 has no effect until R11 is installed.

Chapter 2

Digital Interface

The digital interface for the EVM is simply the appropriate digital signals from the ADC routed and presented to the 20-pin digital interface connector.

Topic **Page**

2.1 Physical Pinout Description

The TLV2553/6EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW−110−22−F−D−VS−K and TSM−110−01−T−DV−P provide a convenient 10-pin dual row header/socket combination at P3.

This header/socket combination provides access to the digital control and serial data pins of the TLV2553/6. Consult Samtec at www.samtec.com or 1−800−SAMTEC−9 for a variety of mating connector options.

Table 2−1. Digital Control Pinout

Pin Number		Signal	Description
Header	Socket		
P3.1	J3.1	$\overline{CS}$	Chip select selects the device for data transfer.
P3.3	J3.3	SCLK	Data transfer clock
P3.5	J3.5	Reserved	
P3.7	J3.7	Reserved	
P3.9	J3.9	Reserved	
P3.11	J3.11	SDI	Serial data into the device
P3.13	J3.13	SDO	Serial data out of the device
P3.15	J3.15	EOC or $\overline{INT}$/EOC†	Selects either EOC or $\overline{INT}$ − see data sheet for details.
P3.17	J3.17	Reserved	
P3.19	J3.19	Reserved	

† EOC or EOC/$\overline{INT}$ depend upon whether the TLV2553EVM or TLV2556 is installed.

Chapter 3

Power Supply

The TLV2553/6EVM board accepts three power supplies.

- A dual ±Vs dc supply for the dual-supply op-amps and the voltage reference.
- A single 2.7-V to 5-V dc supply for the ADC.

There are two ways to provide these voltages:

- Hook-up the test points on the EVM. The test points are clearly labeled $+V_{CC}$ (2.7 to 5 V), +Vs (up to 18 V depending upon the amplifiers) and –Vs (up to –18 V depending upon the amplifiers).
- Use the power connector P5/J5 and derive the voltages elsewhere.

The pinout for this connector is shown in Table 3–1.

Table 3–1. Power Supply Connector

Signal	P5/J5 Pin Number		Signal
+VA	1	2	–VA
+5VA	3	4	–5VA
AGND	5	6	DGND
+1.8VD	7	8	VD1
+3.3VD	9	10	+5VD

Chapter 4

Getting the Most From Your EVM

TI recognizes that a wide range of prototyping options and software solutions offer additional flexibility and reduce your time to market. Hardware and software offerings from TI help you to get from concept to hardware and software prototype easily.

Topic **Page**

4.1 Additional Hardware Options

In general, there are three hardware directions that the user can take with the EVM.

4.1.1 Stand-Alone EVM

The EVM can be used on its own. Using the EVM in this manner obliges the user to provide a custom digital interface between the EVM and a host system. Users are entirely responsible for ensuring proper timing requirements are met in addition to providing any glue logic necessary. Users must also provide the necessary analog interface and supply power to the EVM.

4.1.2 DSP Interface

Depending upon the DSP that the user chooses, there are a number of TI DSKs available. DSKs are ***D***SP ***S***tarter ***K***its, and provide users with a DSP starter system. They contain all the necessary hardware and software to quickly begin prototype construction.

> For example, the TMS320C6711™ DSP Starter Kit includes the DSK hardware, a parallel port cable to connect to a PC, a 5-V universal power supply and a Code Composer Studio™ CD-ROM containing all the necessary software.

Each family of DSKs provide different physical interface options. The interfaces enable address, data and control signals to be decoded and used by mezzanine-level cards (such as EVMs).

To connect this EVM to any DSK requires selection of the correct interface card. Generally the procedure is outlined below.

- ❑ Select which DSP you wish to use.
- ❑ Select appropriate DSK.
- ❑ Select suitable interface card.

4.1.3 MSP430 Microcontroller Interface

TI also offer a range of low-power microcontrollers that have an SPI interface. You can check-out these devices and order evaluation modules at www.ti.com

The TLV2553 ADC and TLV2556 ADC support SPI mode 0 transfers.

4.2 Software Development

Texas Instruments is aware that software development time is critical. When using TI DSPs (DSKs), there are a number of options that improve development times.

4.2.1 Plug-Ins

Accelerate software development by using plug-ins developed by TI for this EVM and available at www.ti.com.

Chapter 5

TLV2553/6 EVM Bill of Materials

The following table contains a complete Bill of Materials for the TLV2553 and TLV2556 EVM.

Item No.	Qty	Value	Ref Des	Description	Vendor	Part number
1	4	0R	R12, R14, R17, R20	1/4W 1206 chip resistor	Panasonic	ERJ-8GEY0R00V
2	1	100R	R13	1/4W 1206 chip resistor	Panasonic	ERJ-8GEYJ101V
3	12	33R	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R15, R19	1/4W 1206 chip resistor	Panasonic	ERJ-8GEYJ330V
4	1	10 pF	C23	Multilayer ceramic−0805 size	Panasonic	ECJ-2VC1H100D
5	11	27nF	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C22	Multilayer ceramic−0805 size	Panasonic	ECJ-2VB1H273K
6	5	0.1 μF	C1, C2, C16, C19, C24	Multilayer ceramic−0805 size	Panasonic	ECJ-2VB1E104K
7	1	1 μF	C20	Multilayer ceramic−0805 size	Panasonic	ECJ-2YB1A105K
8	1	10 μF	C18	Polarized capacitor	Panasonic	ECS-T1CX106R
9	4	10 μF	C13, C14 C17, C21	Panasonic aluminum C size surface mount	Panasonic	ECE-V1CA100SR
10	1		W1	2 Position jumper, 0.1” spacing	Samtec	TSW-102-07-L-S
11	5		W2, W3, W4, W5, W6	3 Position jumper, 0.1” spacing	Samtec	TSW-103-07-L-S
12	1		P5	10 Pin header	Samtec	TSM-105-01-T-DV-P
13	1		J5	10 Socket strip	Samtec	SSW-105-22-F-D-VS-K
14	4		P1, P2, P3, P4	20 Pin header	Samtec	TSM−110−01−T−DV−P
15	4		J1, J2, J3, J4	20 Socket strip	Samtec	SSW-110-22-F-D-VS-K
16	3		FB1, FB2, FB3	Fair−Rite SM beads #24−44447	Fair−Rite	2744044447

Item No.	Qty	Value	Ref Des	Description	Vendor	Part number
	2		R16, R21	Surface mount resistor	*	*
	1		C15	Multilayer ceramic−0805 size	*	*
	2		R11, R18	1/4W 1206 Chip resistor	*	*
	1		RV1	Bourns 32X4W series 5T Pot	*	*
17	1			TLV2553/6 PWB		6432156
18	2		U1, U4	Precision single amplifier	Texas Instruments	OPA132UA
19	1		U3	REF 02 Voltage regulator	Texas Instruments	REF02BU
20	1		U2	TLV2553. 12 bit, 11-channel serial ADC	Texas Instruments	TLV2553IPW
			U2— Alternative	TLV2556, 12 bit, 11-channel serial ADC	Texas Instruments	TLV2556IPW
21	3		$+V_{CC}$, $+V_S$, $-V_S$	Test point−single 0.025” pin	Keystone Electronics	5000
22	2		AGND, DGND	Turret terminal test point	Cambion	180-7337-02-05
23	5	See assy dwg for details		Shunt	Samtec	

Chapter 6

TLV2553/6 EVM Board Layout and Schematic

This chapter contains the TLV2553/6 EVM board layout drawings and the schematic.

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6.1 TLV2553/6 EVM Layout Details

Figure 6−1. Top Tracking Layer

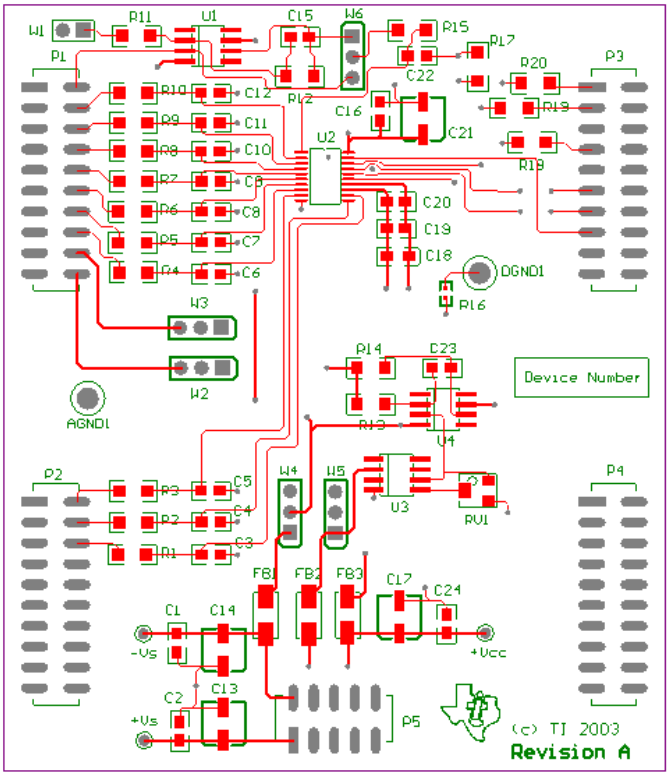


Figure 6–2. Internal Power and Ground Layers

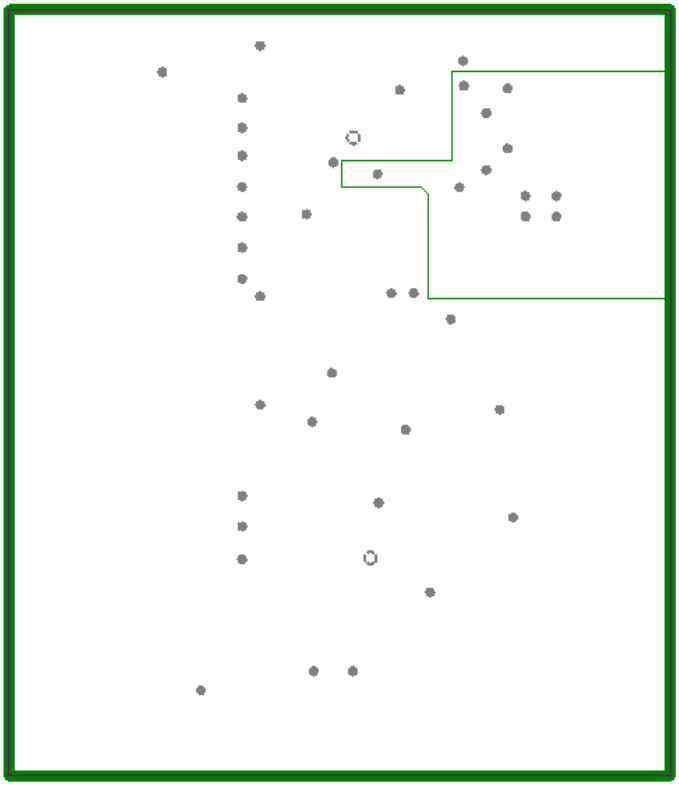
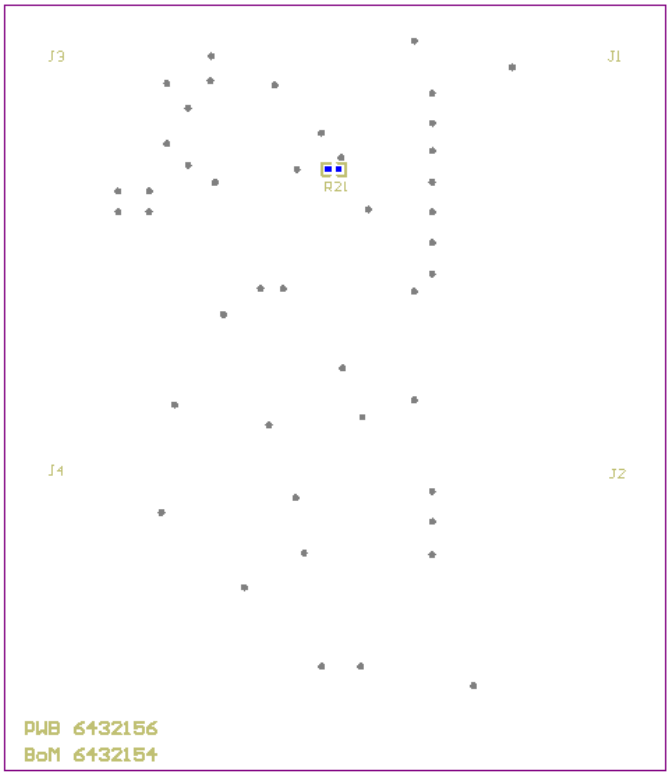


Figure 6–3. Bottom Tracking Layer



6.2 TLV2553/6 EVM Schematic

The TLV2553/6 EVM schematic is attached on the following page.

Revision History		
REV	ECN Number	Approved

W1 R11 Not Installed C15 Not Installed R12 0R AGND

CH0 W6 R15 33R C22 27nF AGND

Amplifier +Supply Amplifier -Supply U1 -In +In Output

+Vcc_A C16 0.1uF C21 10uF AGND

P1: CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 REF- REF+

P2: CH8 CH9 CH10

R10 33R C12 27nF AGND
R9 33R C11 27nF AGND
R8 33R C10 27nF AGND
R7 33R C9 27nF AGND
R6 33R C8 27nF AGND

CH6 R5 33R C7 27nF AGND
CH7 R4 33R C6 27nF AGND
CH8 R3 33R C5 27nF AGND
CH9 R2 33R C4 27nF AGND
CH10 R1 33R C3 27nF AGND

U2 TLV2553 / 56
AIN0 AIN1 AIN2 AIN3 AIN4 AIN5 AIN6 AIN7 AIN8 AIN9 AIN10
Vcc GND
CS* I/O CLK DATA_IN DATA_OUT EOC REF+ REF-
CS* BCLK DATA_IN DATA_OUT EOC REF_P REF_M

P3: CS* R20 0R CLKX CS* R18 Not Installed FSX R19 33R DGND

P4: HEADER 10 X 2

REF_P C19 0.1uF C20 1uF C18 10uF REF_M
W2 REF+ VREF+ REF- W3 AGND

R13 100R C23 10pF
Amplifier +Supply Amplifier -Supply U4 -In +In Output R14 0R VREF+

U3 REF02 Vin Vo Trim GND Temp NC NC NC +Vs_A RV1 Not Installed

+Vcc FB3 +Vcc_A W5 Amplifier +Supply C24 0.1uF C17 10uF AGND
+Vs FB2 +Vs_A C2 0.1uF C13 10uF AGND
-Vs FB1 -Vs_A W4 Amplifier -Supply C1 0.1uF C14 10uF AGND

P5

R21 Not Installed R16 Not Installed R17 0R AGND1 DGND1 AGND DGND

Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	TLV2553 Revision A

12500 TI Boulevard. Dallas, Texas 75243

Title: TLV2553 / 56 Evaluation Module

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